SPECIFICATION

Please replace the title with the following:

A FLASH MEMORY CELL WITH DRAIN AND SOURCE FORMED BY DIFFUSION OF A DOPANT FROM A SILICIDE ~~FABRICATION METHOD~~.

Please replace the second paragraph starting on line 15 of page 6 with the following:

Figure 3 is a block diagram illustration of a flash memory cell 300 in accordance with one embodiment of the present invention. Flash memory cell 300 includes control gate 310, charge storing region 315 (e.g., a floating gate), insulation region 317 (e.g., an oxide region), source 320, drain 330, sidewalls 331, well region 350 (e.g., a substrate) and current conducting channel 375. In one exemplary implementation, a source extension region 221 and drain extension region 231 are formed by very shallow implantation. Source 320 and drain 330 are formed by implantation of a dopant (e.g., arsenic) and diffusion of a dopant from silicide layer 170 (e.g., a cobalt silicide layer). Control gate 310 is coupled to insulation region 317 which is coupled to floating charge trapping region 315 and well region 350. Well region 350 is coupled to source 320 and drain 330. For ease of use and convention, charge storing region 315 and semi-permeable insulating region 317 are referred to as a floating gate and an oxide region respectively, but are not necessarily limited to these implementations.